David W. Parent
Full Professor
Department of Electrical Engineering
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Professional Preparation:

University of Connecticut, Electrical Engineering, B.S.	1992
University of Connecticut, Electrical Engineering, M.S.	1996
University of Connecticut, Electrical Engineering, Ph.D.	1999

Appointments:

Full Professor, Electrical Engineer, San Jose State University,	2011-present
Associate Professor, Electrical Engineering, San Jose State University,	2005-2011

19. X. G. Zhang, P. Li, G. Zhao, D. W. Parent, F. C. Jain, J. E. Ayers: *Removal of threading dislocations from patterned heteroepitaxial semiconductors by glide to sidewalls*. Journal of Electronic Materials 11/1998; 27(11):1248-1253., DOI:10.1007/s11664-998-0078-3
20. D. W. Parent, S. Kalisetty, X. G. Zhang, G. Zhao, W. Zappone, J. Robinson, E. Heller, J. E. Ayers, F. C. Jain: *A comparison of ethyl iodide and hydrogen chloride for doping ZnSe grown by photoassisted MOVPE*. Journal of Electronic Materials 06/1997; 26(6):710-714., DOI:10.1007/s11664-997-0220-7
21. X.G. Zhang, S. Kalisetty, J. Robinson, G. Zhao, D.W. Parent, J.E. Ayers, F.C. Jain: *Structural properties of ZnSySe1 - Y/ZnSe/GaAs(0 0 1) heterostructures grown by photoassisted metalorganic vapor phase epitaxy*. Journal of Electronic Materials 06/1997; 174(1):726-732., DOI:10.1016/S0022-0248(97)00065-1
22. X. G. Zhang, S. Kalisetty, J. Robinson, G. Zhao, D. W. Parent, J. E. Ayers, F. C. Jain: *Structural Properties of ZnSSe/ZnSe/GaAs (001) Heterostructures Grown by Photoassisted Metalorganic Vapor Phase Epitaxy*. Journal of Electronic Materials 02/1997; 26(6)., DOI:10.1007/s11664-997-0218-1

Conference Proceedings:

1. David W. Parent, Jinny Rhee: *Long term study of prior GPA, prerequisite physics success, class size, and directed self-placement on student success in an introduction to circuit analysis course.* FIE 2019, Paper Accepted
2. David W. Parent: *Pilot study of a workshop designed to improve student learning outcomes in a junior level circuits and signals course.* FIE 2019, Paper Accepted
3. David W. Parent: *Development of a placement exam to increase student success in a junior level circuits and systems class*. FIE 2018; 10/2018
4. David W. Parent: *Examination the impact of various factors on student success in an introduction to circuit analysis course*. FIE 2018; 10/2018
5. David Wahlgren Parent, Patricia Backer: *Integration of an electrical engineering capstone course with social justice and global studies*. FIE 2018, San Jose CA; 10/2018
6. David Parent, Eric Basham: *A Neuromorphic Quadratic, Integrate, and Fire Silicon Neuron with Adaptive Gain*. EMBC, Honolulu Hawaii; 07/2018
7. David W. Parent: *Novel gateway stay/add policy used to increase student success rates in an introductory circuits class*. 2017 IEEE Frontiers in Education Conference (FIE); 10/2017, DOI:10.1109/FIE.2017.8190600
8. David W. Parent: *Improvements to an Electrical Engineering Skill Audit Exam to Improve Student Mastery of Core EE concepts*. Microelectronic Systems Education, 2009. MSE '09. IEEE International Conference on; 08/2009, DOI:10.1109/MSE.2009.5270829

9. David W. Parent, Eric J. Basham: *A Course for Designing Transistors for High Gain Analog Applications*. University/Government/Industry Micro/Nano Symposium, 2008. UGIM 2008. 17th Biennial; 08/2008, DOI:10.1109/UGIM.2008.27
10. D.W. Parent: *A 2-Mask NMOS Process Design Fabricate and Test Module for Use In Microelectronics Instruction and Process Development*. University/Government/Industry Microelectronics Symposium, 2006 16th Biennial; 07/2006, DOI:10.1109/UGIM.2006.4286353
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