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PROFESSIONAL BIOGRAPHY:

Dr. Chang Choo is currently Professor of Electrical Engineering and Director of DSP/FPGA Laboratory at San Jose State University, San Jose, California. He was Se-2(o)2(r)ecurrentem of-based DSP systemsputer architecture. He design, including video/audio compression, wireless communications and adaptive filtering. He has over 80 journal and conference publications and 7 patents in these areas. He was a member of Technical Committee with several professional conferences including SPIE, DesignCon, and DSP World/ICSPAT. He was a consultant for various companies including Philips Semiconductor, National Semiconductor (acquired by Texas Instruments), Ricoh Innovations and Skybox (acquired by Google). Dr. Choo received his PhD in computer and systems engineering from Rensselaer Polytechnic Institute, Troy, NY.

[8] Philips Semiconductor, COMPARATIVE PERFORMANCE EVALUATION OF PHILIPS TRIMEDIA PROCESSOR, June 1, 1997 - August 31, 1997, $30,000.
[9] FutureTel/Innovacom, MPEG-2 Encoder ASIC Design, May 1996 - September 1996, $25,000.
[10] National Semiconductor, C50-Based NSV (National Semiconductor Video) Compression System Development, December 1995 - June 1996, $15,000.
[11] National Semiconductor, Performance Evaluation of H.26P TMN4/SAAC (Very Low Bitrate Video Coding Standard for Public Switching Telephone Network), November 1994 - June 1995, $19,000.
[12] National Science Foundation, Developing Advanced Digital Design Laboratory Using Field Programmable Gate Array Development Systems, September 1992 - February 1995, $66,832 (50% non-NSF contribution).
[13] Texas Instruments, Digital Signal Processor Equipment Grant, January 1990, $100,000.

SELECTED COURSES TAUGHT:

FPGA Design of Video and Image Processing Algorithms (1-day short course given in 2010 and 2009 SPIE Electronic Imaging Conference), FPGA DSP Systems Design (4-day short course to engineers and managers, as well as semester-long graduate course); Advanced VLSI Design for DSP and Communications; Logic Circuit Design; Digital Design Using HDL; Digital Signal Processing; Advanced Computer Architectures; Programmable Architectures for DSP (TI DSP Processor Architectures); Digital Image Processing; Microprocessor Systems Design; Advanced Topics in Computer Vision, Graphics and CAD.

SELECTED PROFESSIONAL SERVICES:

[1] Associate Editor, Journal of Real-Time Image Processing, Springer, February 2013-January 2015.
[2] Member of Program Committee, Real-Time Image and Video Processing, IS&T/SPI.002(I)20(.002 I)(b)2(er)-2(o96 7

[3] "Hashing-Based Vector Quantization," U.S. Patent Nos. 5,832,131 (1998) and 5,991,455 (1999) (with X. Ran).
[4] "Syntax Based Arithmetic Coder and Decoder," U.S. Patent No. 5,587,710, 1997 (with X. Ran, et al.).

SELECTED EXPERT WITNESS ENGAGEMENT

Parties: SanDisk Corp. v. LSI Corp./Agere Systems, Inc.
Time Frame: Spring 2010
Primary Contact: Judge Hon. William Alsup
Contact's Firm: U.S. District Court, Northern District of California, San Francisco Division
Contribution: Rule 706 Expert (Expert appointed by Federal Court)
Relevant expertise: MP3 and MPEG-2 audio and video compression software and hardware

Parties: Civolution B.V. v. Doremi Labs, Inc.
Time Frame: Spring 2015
Primary Contact: Dr. Cliff Maier, Esq.
Contact's Firm: Mayer Brown LLP
Contribution: Expert Witness
Relevant expertise: FPGA hardware and HDL for digital watermarking for video server

SELECTED PUBLICATIONS

[1] "FPGA-Based Hardware Accelerator for Feature Extraction in Automatic Speech Recognition," Int. J. lnfo. Commun. Converg. Eng. 13(3): 145-151, Sep. 2015 (with Y.U. Chang and I.Y. Moon).
[2] "Novel Write request handling for Static Wear Leveling in Flash Memory (SSD) Controller," Int. J. lnfo. Commun. Converg. Eng. 11(3): 147-154, Sep. 2013 (with P. Gajipara and I.Y. Moon).
[3] "FPGA Design of a Real-Time Edge Enhancing Smoothing Filter," IS&T/SPIE Electronic Imaging, Burlingame, California, Feb. 3-7, 2013 (with N. Pandya).
[4] "An FPGA-Based Embedded Wideband Audio Codec System," 19th international Conference

III International Conf. Acoustics, Sound, and Signal Processing, Salt Lake City, Utah, pp.3301-3304, May 7-11, 2001 (with H. Elabd).

[13] “Designing High-Performance Echo Canceller for VOIP,” DSP Engineering Mag., vol.2, no.1, pp. 12-26, 2000.

[14] “Constrained Variable-Bit-Rate Control Algorithm for MPEG-2 Encoder,” Proc. SPIE, vol. 3974, pp.133-143, Image and Video Communications and Processing 2000, B. Vasudev; T.R. Hsing; A.G. Tescher; R.L. Stevenson; Eds. (with D. Zhang).

[15] “Optimization of 2D median filtering algorithm for VLIW architecture,” Proc. SPIE, vol.3970, pp. 70-79, Media Processors 2000, S. Panchanathan; V.M. Bove; S.I. Sudharsanan; Eds. (with M. Tang).

[16] “Design and Implementation of Digital FIR Filters Using Altera FIR Compiler,” DSP and Multimedia Magazine, 1999.

[17] “Video Applications for Distributed Arithmetic,” tutorial workshop paper, ICSPAT-99, Orlando, Florida, November 1999.

[18] “Syntax-Based Arithmetic Video Coding for Very Low Bitrate Visual Telephony,” Proc. IEEE Intern. Conf. Image Processing, Washington, DC, pp.II410-II413, Oct. 22-25, 1995 (with X. Ran).

[19] “Evaluation of Design Parameters for a Cache Vector Quantization System,” Proc. First IEEE Conference on Image Processing, Austin, Texas, pp. 129-133, Nov. 13-16, 1994 (with N. M. Nasrabadi).

[20] H.26P/TMN2 NSC: National Semiconductor, 1998 (with F. Jin).